

22-22-00  
A  
FISH & RICHARDSON P.C.

4225 Executive Square  
Suite 1400  
La Jolla, California  
92037

Telephone  
858 678-5070

Facsimile  
858 678-5099

Web Site  
www.fr.com

Frederick P. Fish  
1855-1930

W.K. Richardson  
1859-1951

February 16, 2000

Attorney Docket No.: 08305/064001/99-02

**Box Patent Application**

Assistant Commissioner for Patents  
Washington, DC 20231

Presented for filing is a new patent application claiming priority from a provisional patent application of:

**Applicant: SANDOR L. BARNA AND ERIC R. FOSSUM**

**Title: TECHNIQUE FOR FLAGGING OVERSATURATED PIXELS**

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	<u>Pages</u>
Specification	14
Claims	4
Abstract	1
Declaration	[To be Filed at a Later Date]
Drawing(s)	5

Enclosures:

— Postcard.

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/120,423, filed February 16, 2000.

This application is entitled to small entity status. A small entity statement will be filed at a later date.

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL528185325US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit

February 16, 2000

Signature

Rich Donovan

Typed or Printed Name of Person Signing Certificate



BOSTON  
DELAWARE  
NEW YORK  
SILICON VALLEY  
SOUTHERN CALIFORNIA  
TWIN CITIES  
WASHINGTON, DC

02/16/00



FISH & RICHARDSON P.C.

Assistant Commissioner for Patents

February 16, 2000

Page 2

Basic filing fee	\$0
Total claims in excess of 20 times \$9	\$0
Independent claims in excess of 3 times \$39	\$0
Fee for multiple dependent claims	\$0
Total filing fee:	\$0

No filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE**, to deposit account 06-1050, referencing the attorney document number shown above. A duplicate copy of this transmittal letter is attached.

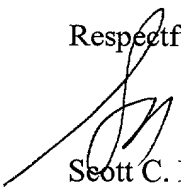
If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (858) 678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

SCOTT C. HARRIS  
Fish & Richardson P.C.  
4225 Executive Square, Suite 1400  
La Jolla, CA 92037

Respectfully submitted,

  
Scott C. Harris  
Reg. No. 32,030  
Enclosures  
SCH/nsg  
10019929

009720-9490960

APPLICATION  
FOR  
UNITED STATES LETTERS PATENT

TITLE:           TECHNIQUE FOR FLAGGING OVERSATURATED  
                  PIXELS

APPLICANT:     SANDOR L. BARNA AND ERIC R. FOSSUM

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL528185325US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit February 16, 2000

Signature

Rich Donovan

Typed or Printed Name of Person Signing Certificate

# TECHNIQUE FOR FLAGGING OVERSATURATED PIXELS

## CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of the U.S. Provisional Application No. 60/120,423 entitled TECHNIQUE FOR FLAGGING OVERSATURATED PIXELS filed on February 16, 1999.

## TECHNICAL FIELD

This invention relates to digital imaging sensors, and more particularly to active-pixel sensors.

## BACKGROUND

Charge coupled devices (CCD) have traditionally been the imagers of choice for high quality imaging devices due to their high sensitivity and fill-factor. However, the standard CCD formation process often is incompatible with CMOS processing. Accordingly, it is impractical to integrate on-chip signal processing electronics in a CCD imager and the signal processing electronics must be provided off-chip.

CCDs are essentially electronic analog shift registers. CCDs include rows of photodetectors that act essentially as capacitors. Each pixel converts light energy into a charge, and then transfers that charge sequentially across a row of pixels into a single charge amplifier. This operation

requires nearly perfect charge transfer efficiency, resulting in slow readout rates and relatively large power requirements.

Active pixel sensor (APS) devices are described in U.S. Patent No. 5,417,515. These include an array of pixel cells  
5 that convert light energy into electrical signals. Each pixel includes a photodetector and one or more active. APS imaging devices are compatible with complementary metal oxide semiconductor (CMOS) technology.

Conventional CMOS imaging devices can be prone to  
10 producing artifacts in the resulting image. Artifacts are areas in the image that correspond to areas of the sensor that have been exposed to extremely high light levels. Artifacts appear black in the image when in fact they should be the brightest objects in the image.

15 Artifacts are produced by highly oversaturated pixels in the APS. Oversaturated pixels are pixels that are exposed to more light energy than the pixel's photodetector can absorb during exposure time.

APS devices can be operated in a double-sampling mode, in  
20 which the difference between the reset voltage and the signal voltage determines the brightness of the pixel. At zero light level, the signal value does not drop from the reset voltage and hence the difference voltage is zero, producing a black

pixel. As the signal voltage drops, the difference voltage increases and the pixel brightens.

At high light levels, the signal voltage saturates at a saturation voltage  $V_{sat}$ .

5       The reset voltage also drops in response to incident light but at a much lower rate than the signal voltage. At very high light levels, the reset voltage begins to decrease significantly. At extremely high light levels reset voltage  $R$  will also saturate at  $V_{sat}$ . At this point, the difference  
10       voltage is zero, which produces a black pixel.

      This is mainly a problem in very high contrast images. The extreme brightness of the sun will cause this effect in virtually all CMOS imagers, even at very short integration times. This is a disconcerting effect in outdoor imaging  
15       situations, in which the sun is often accidentally included in the field of view.

      FIG. 1 illustrates such a situation in a digital image 10 produced using a conventional APS CMOS imager. The presence of the sun 12 in the image produces an artifact 14 in which  
20       the center of the sun appears black.

## SUMMARY

According to an embodiment of the invention, an active pixel sensor (APS) includes a pixel with a photodetector that converts a charge on the photodetector into a voltage, a sample and hold element for sampling and storing a signal voltage from the pixel during a readout operation, and a comparator for comparing the signal voltage to an adjusted saturation voltage to determine if the pixel is saturated.

According to another embodiment of the invention, a saturation flag is associated with the pixel and stored if the adjusted saturation voltage exceeds the signal voltage.

According to yet another embodiment of the invention, a difference voltage is determined for the pixel from the read out signal voltage and reset voltage. An analog-to-digital converter is provided for converting the difference voltage into a digital difference value. This digital difference value is replaced with a maximum digital value for pixels in the APS in the event a saturation flag is detected for that pixel.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

## DESCRIPTION OF DRAWINGS

FIG. 1 is a digital image including an artifact produced in the center of the sun caused by oversaturated pixels.

FIG. 2 is a schematic diagram according to an embodiment  
5 of the invention.

FIG. 3 is a chart showing the response of voltage levels to incident light levels according to the embodiment of FIG. 2.

FIG. 4 is a schematic diagram showing another embodiment  
10 of the invention including digital processing circuitry.

FIG. 5 is a schematic diagram showing another embodiment of the invention in which the APS has a column-parallel architecture.

Like reference symbols in the various drawings indicate  
15 like elements.

## DETAILED DESCRIPTION

Oversaturated pixels in an active pixel sensor (APS) imaging device can produce artifacts in the resulting images in high contrast situations. Artifacts are objects in the  
20 image that appear black, but in fact should be the brightest objects in the image.

According to the present embodiment, oversaturated pixels in an APS pixel array are flagged during readout. The



saturation flag can be used to identify oversaturated pixels and replace the value read out from oversaturated pixels with a predetermined maximum value corresponding to a maximum brightness for the pixels in the image. This removes the artifacts in the resulting image, and the pixels in the APS array that receive the most light appear brightest in the images that are produced.

FIG. 2 illustrates an embodiment of the invention. An APS 20 includes an array of independently addressable pixels arranged in n rows and m columns. An independently addressable pixel 22 in a row 24 includes a photodiode 26, a reset transistor 28, a source-follower output transistor 30, and a row select transistor 32. Pixels in each row are connected to a column 34. The bottom of each column of pixels has a load transistor 36 at a voltage  $V_{ln}$ , an output branch 38 to store the signal level for readout, an output branch 40 to store the reset level for readout, and an output branch 42 to store the signal level for a comparison to determine whether the pixel is saturated.

The signal branch 38 has a signal sample and hold (SH) element. This can include a sampling switch 46 and a holding capacitor 48. The reset branch 40 includes a sampling switch 52 and a holding capacitor 54. The comparator branch 56 includes a sampling switch 58 and a holding capacitor 60.

Comparator branch 42 is connected to an input node 62 of a comparator device 64. The other input node 66 of comparator 64 is connected to an analog voltage,  $V_{adj}$ , that is adjusted to set a minimum signal level.

5       The output of comparator 64 is connected to a latch 70 to latch the comparator output level after the comparison.

These readout and comparator circuits can be common to entire column 34 of pixels.

Each photodetector 26 in each pixel 22 in the array  
10       converts light energy received in the form of photons into an electrical charge. That charge corresponds to the amount of light that pixel receives prior to a read out function. Readout of pixel 22 for row 24 occurs in three stages: an image integration stage; a signal readout stage; and a reset  
15       stage.

Prior to readout, the voltage on photodiode 26 is reset voltage  $R$ . Reset voltage  $R$  is typically about 3 volts. After the pixel has been selected for readout, this voltage is integrated and decreases in response to incident light.

20       During the integration stage, light energy in the form of photons strikes photodiode 26. Ideally each photon creates an electron-hole pair in the photodiode. Photodiode 26 is designed to limit recombination between the newly formed electron-hole pairs. As a result, the photogenerated holes

and electrons migrate during the integration stage. The photogenerated holes are attracted to the ground terminal of the photodiode, and the photogenerated electrons are attracted to the positive terminal of the photodiode. Each additional  
5 electron attracted to the positive terminal of photodiode 22 reduces the voltage on the photodiode from the reset value R. The integration stage typically takes about 1  $\mu$ sec.

During the signal readout stage, the resultant signal voltage S on photodiode 26 is sampled onto signal branch 44.  
10 In a fully integrated pixel, corresponding to a brightest pixel in the image, the signal voltage S is about 1.5 volts.

During the reset stage, the value of the photodiode is reset to reset voltage R and this value is sampled onto the reset branch 42. The reset operation typically takes about 1  
15  $\mu$ sec.

The sensed light level read out from the pixel, that is the number of photons incident on the photodetector, is determined by calculating the difference between the reset level R and the signal level S.

20 FIG. 3 illustrates the response of the signal voltage S, reset voltage R, and a difference voltage (R-S) to an incident light level. Region I represents the normal operating range of a pixel. At a zero incident light level 100, a pixel in

the resultant image is black. At a high incident light level 102, a pixel in the resultant image has a brightest value.

At high incident light level 102, photodetector 26 becomes unable to absorb additional photons during the  
5 integration period and saturates. According to the present invention, a saturation flag 80 is set for pixel 22 if photodiode 26 is saturated.

Returning to FIG. 2,  $V_{adj}$  is set slightly above  $V_{sat}$  which is typically about 1.5 volts. In operation, the signal  
10 voltage  $S$  sampled onto signal branch 38 is also sampled onto comparator branch 42 during signal readout.

If signal voltage  $S$  is greater than  $V_{adj}$ , comparator 64 output is LOW.

Signal voltage  $S$  will be less than  $V_{adj}$  for all light  
15 levels exceeding an incident light level 104 in Region I of FIG. 3. If signal voltage  $S$  is less than  $V_{adj}$ , the comparator output is HIGH, which represents a saturation flag 80.

The output of the comparator is stored in latch 70. The  
20 latch is enabled during column readout by a column select transistor 82 and the value stored in the latch fed to the downstream column circuitry. Thus, for all incident light levels above incident light level 104, pixel 22 will have an associated saturation flag 80.

According to the present embodiment, the APS CMOS device is a camera-on-a-chip device that includes on-chip analog-to-digital conversion (ADC) circuitry 110, as shown in FIG 4. The ADC circuitry is contained in a digital block 112. Analog signals read out from a pixel are converted to digital signals which are processed in the digital block 112. The digital signals have a maximum value corresponding to the brightest level of the pixels in the image. For example, a maximum digital value for an 8-bit sensor would be 255 (corresponding to binary value "11111111").

The output of latch 70 for column 34 is passed to the digital block along with the analog signal (R-S) during readout of pixel 22. The analog signal is converted to a corresponding digitized value 114. If saturation flag 80 is detected, the digitized value from the ADC is replaced with the maximum digital value, e.g., 255 for an 8-bit sensor.

Thus, the signals read out from pixels receiving incident light levels greater than incident light level 104 in Region I of FIG. 3 will be replaced with the maximum digital value. Accordingly, the corresponding pixels in the image will be the brightest.

Operation of an APS according to the present embodiment will now be explained. For the purpose of illustration, a

pixel exposed to a gradually increasing light level and read out incrementally is considered.

Referring to FIG. 3, at zero incident light level 100, signal voltage S equals reset voltage R. Consequently  
5 difference voltage (R-S) equals zero. The sensor reads a zero value as indicating that the pixel has received no incident light. A zero value produces a black pixel in the resultant image. In Region I, signal voltage S is strongly responsive to the incident light level. As the light level increases,  
10 signal voltage S decreases while reset voltage R remains relatively constant. Thus, difference voltage (R-S) increases, causing the pixel to brighten. Region I corresponds to the photodetector's active region.

According to the present embodiment, pixel 22 operating  
15 in Region I reads out a signal voltage S level greater than V.sat. Since signal voltage  $S > V_{adj}$ , the output of comparator 64 is LOW, indicating that the pixel is operating in the active region, i.e., not saturated. The LOW value is stored in latch 70. During the analog readout of column 34,  
20 the output of the latch is enabled and indicates no saturation flag.

Preferably pixel 22 is flagged prior to photodiode 26 saturating. At signal voltage  $S \approx V_{adj}$ , occurring at incident light level 104 (FIG. 3), the output of comparator 64

may be HIGH or LOW. However, this occurs at the transition between Regions I and II where reset voltage  $R \gg V_{\text{sat}}$ . The presence of artifacts is not a problem where reset voltage  $R \gg V_{\text{sat}}$ .

5        A saturated pixel reads out a signal level equal to  $V_{\text{sat}}$ . Since  $V_{\text{sat}} = \text{signal voltage } S < V_{\text{adj}}$ , the output of comparator 64 is HIGH. The HIGH value is stored in latch 70. During the analog readout of column 34, the output of latch 70 is enabled and indicates a saturated pixel. Saturation flag 10 80 is fed to the column circuitry. The saturation flag is used by the digital processing circuitry to replace the digitized value of the signal fed out from the pixel with the maximum (brightest) digital value for pixels in the image.

15        Ideally, reset voltage  $R$  is constant, However, as shown in Region II of FIG. 3, reset voltage  $R$  drops gradually in response to increasing light levels. This effect is due to pixel 22 still being exposed to light and hence producing electron-hole pairs during the reset stage. Since there is a finite time between setting the photodiode to the reset value and sampling the reset value onto reset branch 40, electrons 20 generated in the photodiode by photons during the reset stage can migrate and reduce the voltage on the positive terminal of photodiode 26.

In Region I of FIG. 3, reset voltage R is relatively constant compared to S. However in Region II, reset voltage R gradually drops while signal voltage S remains constant at V.sat. Consequently, difference voltage (R-S) continues to drop with increasing light levels. In a conventional CMOS imager, the increasingly oversaturated pixel, which should appear to brighten in the image, actually reads out as a darkening pixel.

As shown in Region III, at an extremely high light level 106, reset voltage R will also saturate at V.sat and difference voltage (R-S) will equal zero, representing a black pixel. Regions of such oversaturated pixels produce artifacts in conventional CMOS imagers. FIG. 1 illustrates such an artifact 14 in an image 10 produced with a conventional CMOS imager in which the center of the sun 12 appears black.

In an APS according to the present embodiment, pixels exposed to light levels above light level 104 in Region I of FIG. 3 are flagged with an associated saturation flag 80 and the digital value output for such pixels is replaced with a maximum digital value, e.g., 255 in an 8-bit sensor, thereby preventing artifacts from being produced in the image.

In APS CMOS devices with a column parallel ADC design, each column includes an ADC for conversion of the pixel signal during readout. According to an alternate embodiment shown in



FIG. 5, the comparison function is performed by a pre-existing comparator 124 in the ADC 120 in each column 122, rather than an additional comparator 64, as described above.

According to yet another embodiment, the reset level  
5 reset voltage R is sampled and compared to an analog voltage in Region II of FIG. 3, rather than the signal level S at V.sat.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various  
10 modifications may be made without departing from the spirit and scope of the invention. For example, the photodetector shown in FIG. 2 as photodiode 26 could be any photo-sensing element such as a photogate or pinned photodiode. Also, the digital processing circuitry described as being provided on-  
15 chip could be provided off-chip. Accordingly, other embodiments are within the scope of the following claims.

**WHAT IS CLAIMED IS:**

1 1. An active pixel sensor comprising:

2 at least one pixel comprising a photodetector that  
3 outputs an output level indicative of incoming light;

4 a sample and hold element electrically connected to the  
5 pixel operating to store said output level during a readout  
6 operation;

7 an adjusted saturated voltage source, comprising a node  
8 that provides an adjusted saturation voltage; and

9 a comparator having a first input node operatively  
10 connected to the sample and hold element, a second input node  
11 electrically connected to the adjusted saturation voltage  
12 node, and an output node, said comparator operating to output  
13 a signal indicating whether the adjusted saturation voltage  
14 exceeds the output level from the photodetector.

1 2. The active pixel sensor of claim 1 further comprising a  
2 latch including an input node and an output node, said input  
3 node operatively connected to the output node of the  
4 comparator operating to store a saturation flag in response to  
5 the adjusted saturation voltage exceeding the output level  
6 from the photodiode.

1 3. The active pixel sensor of claim 2 further comprising a  
2 select transistor operatively connected to the output node of

the latch and operating to enable readout of the saturation flag during a readout operation for the pixel.

4. The active pixel sensor of claim 1 wherein the photodetector is a photodiode.

5. An active pixel sensor comprising:  
at least one pixel comprising a photodetector;  
a sample and hold element electrically connected to the pixel and operating to store a signal level on the photodetector during a signal readout operation;  
an adjusted saturated voltage source, comprising a node that provides an adjusted saturation voltage; and  
a comparator having a first input node operatively connected to the sample and hold element, a second input node electrically connected to the adjusted saturation voltage node, and an output node;  
a latch electrically connected to the comparator output node, said latch operating to store a saturation flag in response to the adjusted saturation voltage exceeding the signal level;  
a select transistor operatively connected to the output node of the latch operating to enable readout of the saturation flag during a readout operation for the pixel;

19 a differencing element electrically connected to the  
20 pixel and operating to produce a difference level from the  
21 signal level and a reset level output from the pixel during  
22 the pixel readout operation;  
23 an analog-to-digital converter for converting the  
24 difference level into a difference digital value; and  
25 a digital output selector comprising  
26 a detector operatively connected to the latch output  
27 node,  
28 an input node electrically connected to the analog-to-  
29 digital converter and an output node, and  
30 a switch operating to switch the difference digital value  
31 on the output node to a maximum digital value in response to  
32 the detector detecting a saturation flag.

1 6. The active pixel sensor of claim 5, further comprising a  
2 plurality of pixels arranged in rows and columns.

1 7. The active pixel sensor of claim 6, wherein each column  
2 includes an analog-to-digital converter for converting the  
3 difference level into the difference digital value.

1 8. The active pixel sensor of claim 7, wherein the  
2 comparator is part of the analog-to-digital converter.

1 9. A method for flagging an oversaturated pixel in an active  
2 pixel sensor array, the method comprising:

3 reading a signal voltage from a pixel;  
4 comparing the signal voltage to an adjusted saturation  
5 voltage; and

6 storing a saturation flag in response to the adjusted  
7 saturation voltage exceeding the signal voltage.

1 10. The method of claim 9 further comprising:

2 reading a reset voltage from the pixel;  
3 calculating a digitized value for said pixel from the  
4 reset voltage and the signal voltage;

5 determining whether the pixel has an associated  
6 saturation flag;

7 replacing said digitized value with a maximum digital  
8 value in response to the pixel having an associated saturation  
9 flag.

## ABSTRACT

An active pixel sensor (APS) that includes circuitry to eliminate artifacts in digital images. The APS includes a comparator for comparing a signal level from a pixel to an  
5 adjusted saturation voltage to determine if the pixel is saturated. If the pixel is saturated, an associated saturation flag is stored and used to replace the signal from the pixel with a maximum value corresponding to a brightest pixel in the image.

009720" 54950560

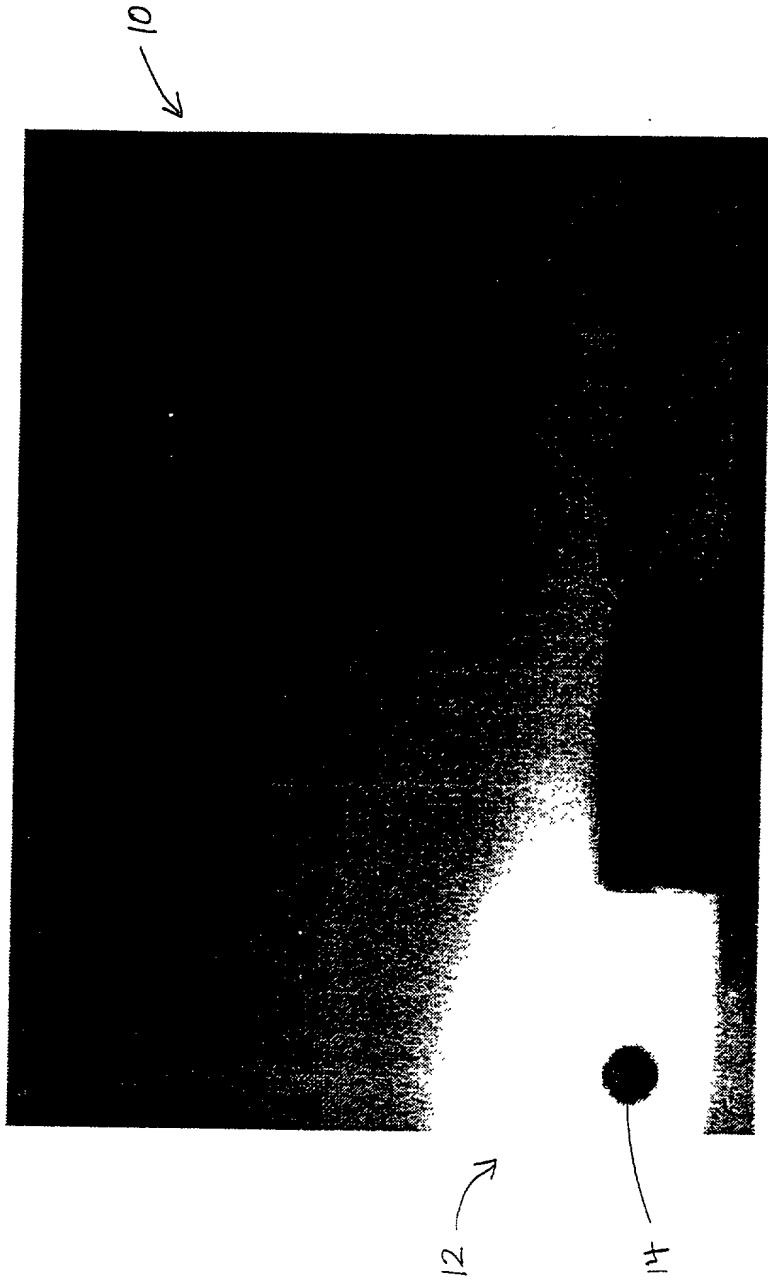


FIG: 1

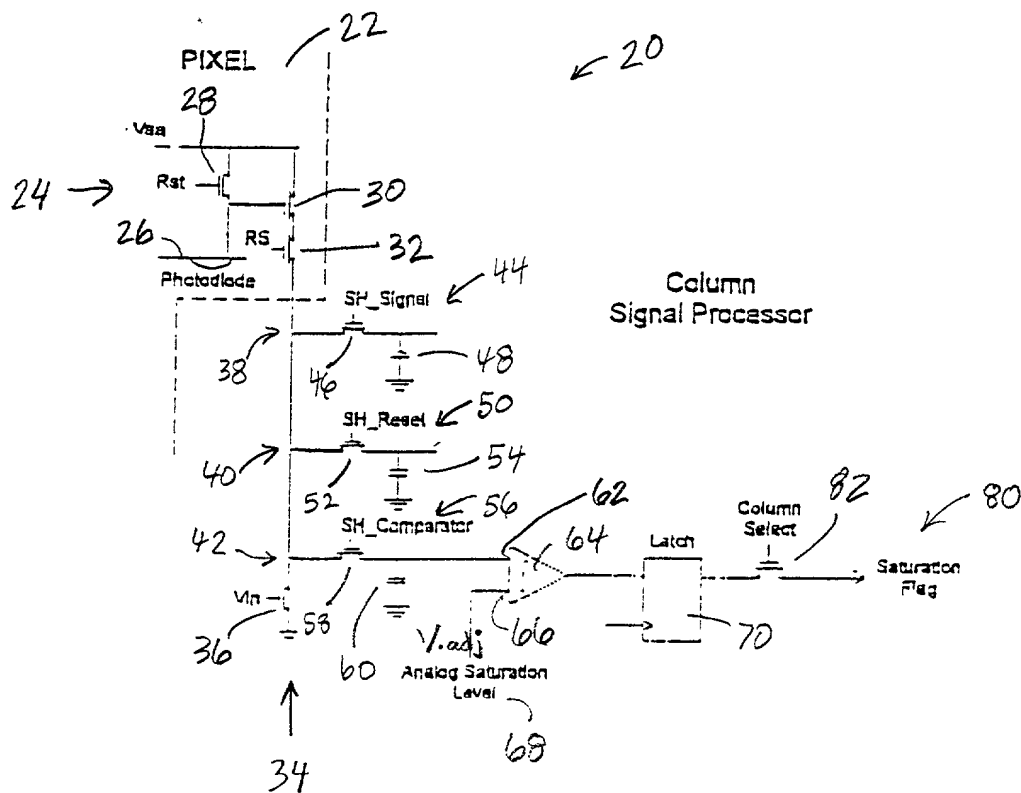


FIG. 2



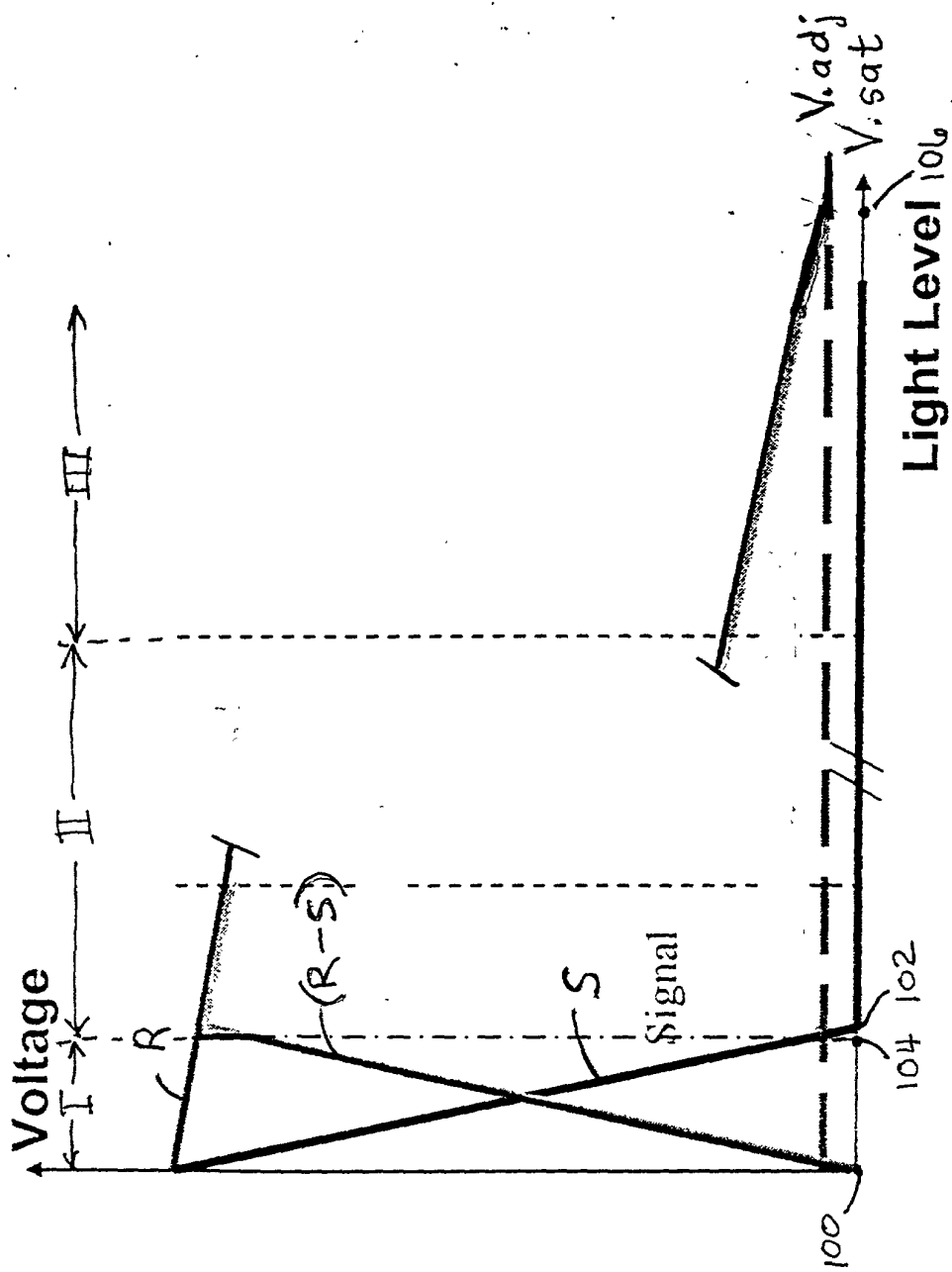


FIG. 3

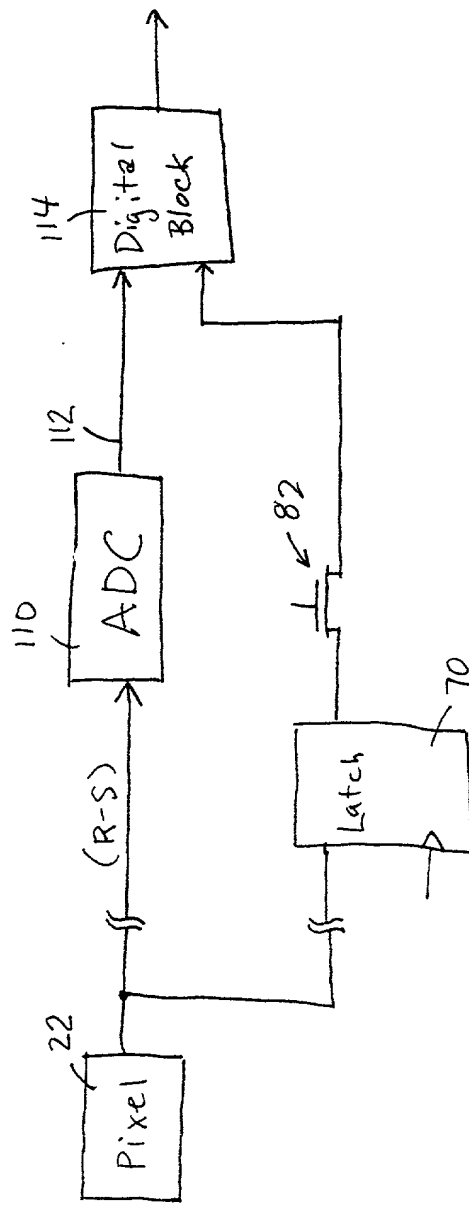


FIG. 4

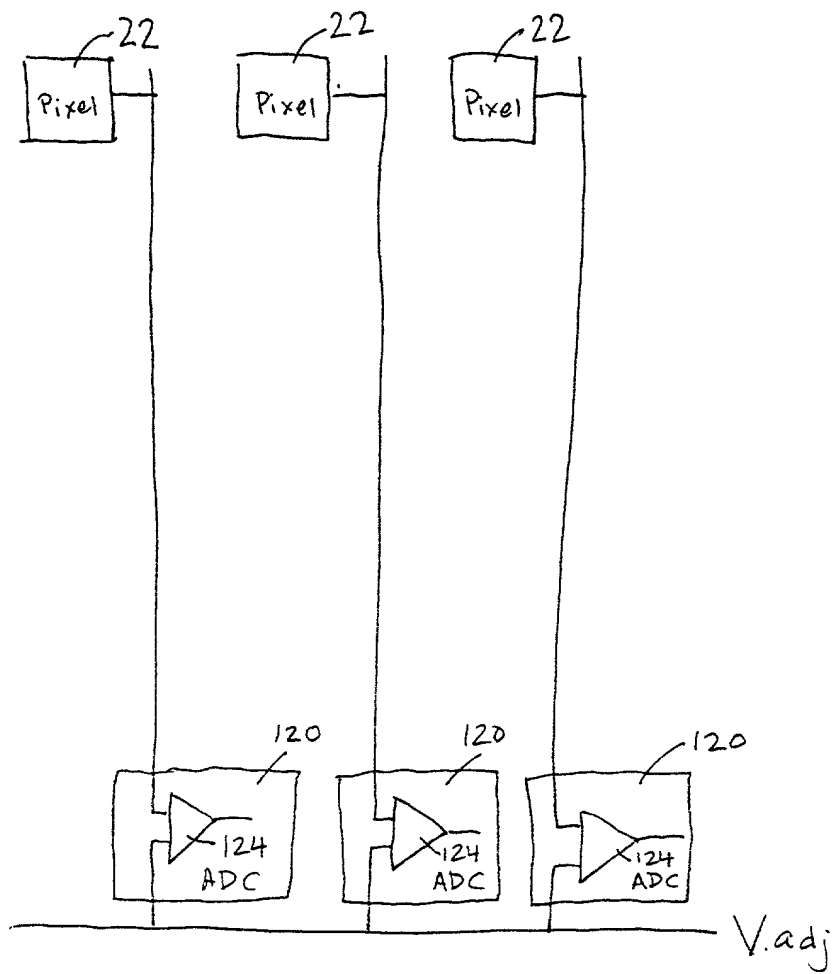


FIG. 5